Application Bulletin AB-13

Method and Advantages of Synchronizing Two RC5051 Converters

Summary

It is becoming more common to build power supplies to power multiple processors. There are limitations in the design of single supplies to provide 30A or more, and so paralleling two supplies is the normal design practice. Synchronizing the two supplies can reduce the number of input capacitors required below what would otherwise be required for two unsynchronized supplies. A cheap synchronization method is featured in this Bulletin, and some test results are shown.

Very High Output Current Converters

A single Pentium II processor can draw up to almost 15A current from its power supply. This current can be best supplied with a single converter based on a Fairchild RC5051. However, when a system contains two or more processors, the currents become so high that additional considerations start to limit the utility of attempting to source the entire current from a single supply:

- When the load current doubles, the I^2R losses in the MOSFET *quadruple*. This necessitates paralleling multiple MOSFETs to get the $R_{DS,on}$ losses down. However, multiple MOSFETs increase the load that the IC must drive, slowing down the gate waveforms and increasing switching losses.
- Controlling the output voltage during a transient becomes very difficult, as adding more output capacitance to the converter starts to add effective ESR because of the trace length.
- The number of input capacitors required becomes quite large, as the input ripple current increases in proportion to the output current.

For all of these reasons, as well as economics, it is desirable to have more than one converter when powering more than one processor. Having multiple converters addresses the first two problems, but does nothing for the third: the number of input capacitors is still large. Having two (or more) converters in parallel has an additional problem:

- Since the two converters are working at almost the same switching frequency, there may be low frequency “beats” between the two of them, which may generate undesirable low-frequency noise.

Synchronizing Converters

The preferred solution to eliminating “beats” between multiple paralleled converters is to *synchronize* them. In its easiest form, this means that one power supply acts as the master, forcing all of the other, slave converters, to run at the master’s switching frequency. Since all of the converters run at exactly the same frequency, there are no beats.

With synchronized converters, it becomes possible to address the question of the large number of input capacitors required. The reason a large number is needed normally is because all of the (high-side, buck) MOSFETs turn on at the same time, and so a large pulse of current is pulled from the capacitors. Suppose, however, that MOSFETs instead turned on alternately, first one set, then the other. In that case, the peak currents pulled from the capacitors would be lessened, reducing also the rms current and thus the number of capacitors required. Spacing the converters apart like this is called *phase-locking*.

Figure 1 shows an inexpensive, low parts-count way of accomplishing this phase-locking. The HIDRV pin of the master RC5051 is used as the locking signal. When the HIDRV pin goes high at the start of the switching cycle, its rising edge triggers a one-shot (the 10KΩ resistor and the two schottkies are used to protect the TTL part from the gate, which goes up to +12V, and may ring below ground). The one-shot is set to produce a pulse of length approximately equal to half the switching period, (1/2) x (1/300kHz) = 1.6μsec. The falling edge of the one-shot’s output is thus delayed one-half cycle. This falling edge triggers the second one-shot to produce a very short pulse (~100nsec). This pulse is coupled in to the timing ramp of the slave RC5051, causing it to begin a new switching cycle, and thus phase locking it.

The only important constraint in this design is that the slave’s natural frequency should be set to approximately 20% lower than the master’s, to account for component tolerances---the locking circuitry only works if the master’s frequency is higher than the slave’s. Note the use of the two 24Ω resistors to couple the signal in to the slave’s ramp; their impedance is low enough to not affect the operation of the slave.

Figure 2 shows the free-running operation of two RC5051 converters: the master runs at 340kHz, while the slave free-runs at 270kHz. Figure 3 shows the same two converters

with the phase-locking circuit attached: both now run at 340kHz. Figure 4 shows the two ramp signals: the slave ramp has a little spike on it from the one-shot's signal being coupled in to it. It is this spike which is resetting the slave's timing ramp, and causing it to run at the same frequency.

Savings

Since the two converters are phased 180° apart, they draw current from the input capacitors at different times, reducing the rms current and thus reducing the number of capacitors required. As an example, suppose that the converters are delivering 30A at 2.0V from a 5V supply. The duty cycle is DC = 40%, and so the average current pulled from the +5V is 30A x 40% = 12A. If a single converter is supplying this power, or if the power is supplied by two separate unsynchronized converters, it (or they) will pull an rms current of:

$$I_{rms} = \sqrt{I_{avg}^{2}(1-DC)+(I_{out}-I_{avg})^{2}DC} = 14.7A$$

Instead, we have two converters, each pulling 15A for 40% DC, phased apart. The rms current in this configuration is

$$I_{rms} = \sqrt{I_{avg}^{2}(1-2\times DC)+\left(\frac{I_{out}}{2}-I_{avg}\right)^{2}\times 2\times DC} = 6A$$

a reduction by more than a factor of two! Thus, the number of input capacitors can be probably cut in half, cutting much more from the cost of the supply than is spent in the inexpensive additional circuitry.

Generalization

Clearly, the same scheme can be generalized to accommodate more converters. For example, four converters powering four processors can be accommodated with three one-shot circuits, set for a delay time of 1/4, 1/2 and 3/4 of the switching period respectively.

Conclusion

Synchronizing converters can be a substantial cost-savings because of the reduction in the input capacitor requirements.

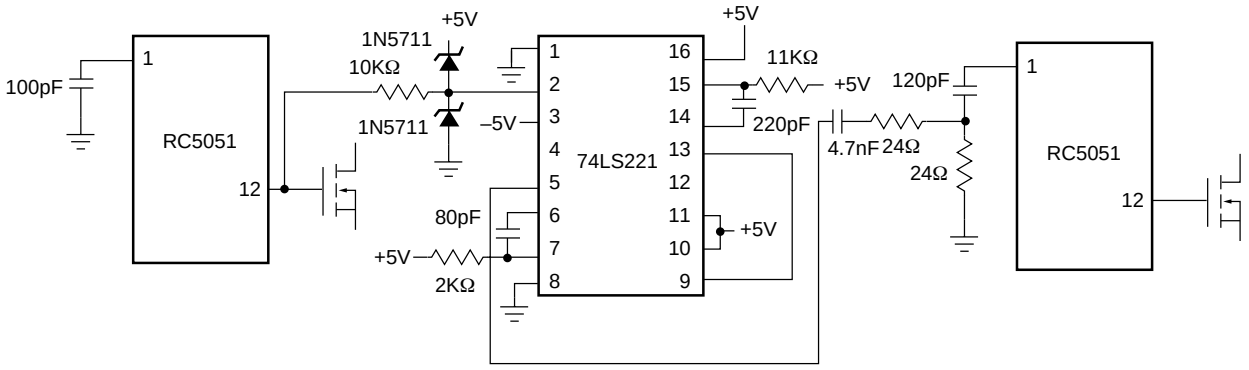

Figure 1. Method of Synchronizing and Phase-Locking Two RC5051 Converters. The RC5051 on the Left is the Master. The 1KΩ and the 1N5817 from the RC5051 to the LS221 are Optional, Depending on Layout.

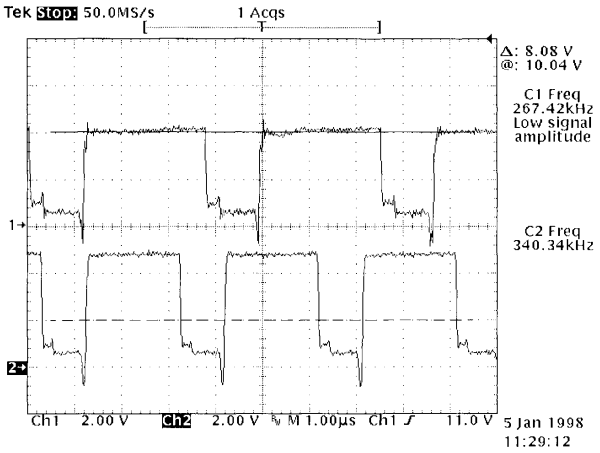

Figure 2. Before Synchronization, the Two Converters Run at Two Different Frequencies.

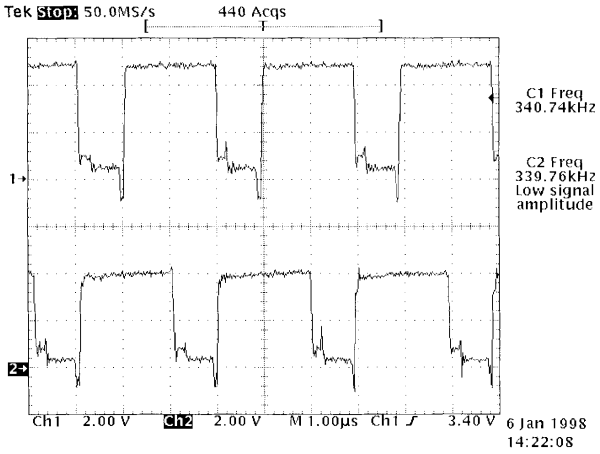

Figure 3. With the Synchronization Circuit Attached, the Two Converters Run at the Same Frequency

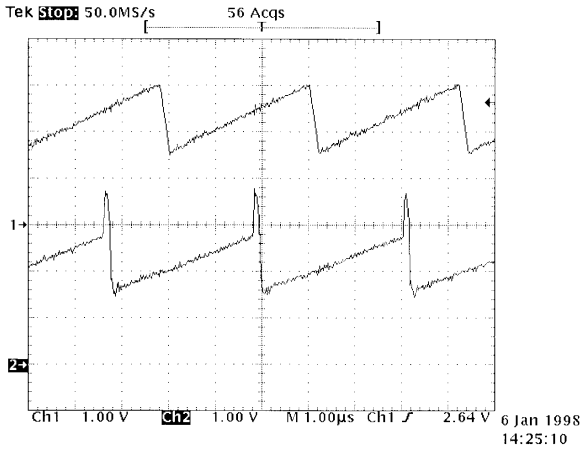

Figure 4. The Two Converters' Ramp Signal. Top: Master. Bottom: Slave.

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